CLASS B OPERATION OF MICROWAVE FETS FOR ARRAY MODULE APPLICATIONS

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Abstract

In addition to the well known class B advantages of high η_{PA} and self turn on for pulsed operation, it is shown herein that class B FET amplifiers have several other important features including:

1) Significantly reduced power dissipation
2) A dynamic range of typically 8-10 dB over which gain is constant and power added efficiency is $>30\%$.
3) Phase behavior (static and dynamic) is comparable to that observed with similar FETs operated class A.
4) Absence of erratic phase behavior during pulse turn-on and turn-off.

These features make class B operation of power FET's very attractive for phased array module applications.

Introduction

The advantages of class B operation of active devices; i.e. high efficiency with attendent low heat dissipation, and self turn-on and turn-off during pulsed operation are well known. In spite of this, the class B mode of operation has not received wide-spread attention for phased array module applications. Two factors are primarily responsible for this lack of interest; 1) concern about transient phase effects during turn-on and turn-off of the applied pulse, and 2) lack of suitable FET's with linear IV characteristics all the way down to pinchoff coupled with a low (2-3 v) gate pinchoff voltage.

This paper presents both CW and pulsed class B measurements on FETs having the aforementioned linear, low voltage pinchoff characteristics. Measurement results confirm the expected high efficiency and also show excellent gain linearity and pulse-to-pulse behavior with less than 6^{o} transient phase variation during turn on/turn off of the applied pulse. These measurements confirm the applicability of class B operation of power FET's for phased array module applications.

Class B Discussion and Measurements

High efficiency is the feature which is most often associated with class B operation.

For array applications, however, this high efficiency with attendent reduced DC input power translates into a far more important and significant reduction in heat dissipation, which can have a dramatic impact in the thermal design of an array. For example, figure 1 illustrates the differences between class A and class B operation of a single stage 1 Watt power amplifier. For the assumed FET and amplifier efficiencies listed (which are resonable as will be seen later), power dissipation drops from 2.42 W for class A operation to 1.26 W for class B operation, a 48% reduction. In spite of the significant reduction in prime power and thermal dissipation, class B operation is usable only if RF performance is also good. Important electrical parameters for array application include 1) range of gain linearity, 2) variation of efficiency with drive level, 3) AM to PM conversion, and 4) interpulse and intrapulse phase variations.

In order to ascertain the feasibility of class B operation for array module applications, a series of CW and pulse measurements were made using a Mitsubishi MGF2124 FET (2400μm gate periphery). The DC characteristics for this FET are shown in Figure 2. Note that this FET has very good pinch-off characteristics, i.e. low pinch-off voltage (2.5-3.0 v), nearly constant gm down to pinch-off, high gate drain breakdown voltage, and low drain current when pinched off, I_D min. A series of CW measurements were made at 8 GHz on three different FETs biased to V_D=6 v and $I_{D\ min}$ = 20 ma with no applied signal (I_{DSS}=650 mA). The associated gate voltages are shown in Figure 3. Figure 3 plots three parameters; e.g. P_{out}, power added efficiency (η_{PA}), and variation of transmission phase as a function of P_{in}. Examination of this figure reveals that all three FETs have peak power added efficiencies between 45 and 48%. Perhaps even more important is the fact that over a fairly wide range of input powers; i.e. +15 to +23 dBm the gain of characteristics are linear ($\approx$5.5 to 6.0 dB gain), power added efficiencies remain above 30%, and transmission phase is essentially constant. This is important for applications where power must be controlled

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linearly; for example, when it is desirable to taper an array to shape the antenna beam. Note further that if some compression is allowable, nearly 1 watt output can be achieved. For an input power of 22 dBm, which corresponds to the maximum power added efficiency point, the AM to PM conversion is only $\approx 2^{o}$/dB.

For reference, it should be noted that over the same input power range; i.e., +15 to +23 dBm, the FET exhibits power added efficiencies varying from 10% to 36% when operated class A and AB. Gain and peak power output are, of course, higher, being 8 dB and 1.3 W respectively.

In order to evaluate transient phase turn on/turn off effects, pulse measurements were also made under class B conditions. Figure 4 shows the input pulse and the excellent amplitude fidelity of the amplified output pulse for two different input power levels. Figure 5 shows the output of a phase bridge which compares the phase of the input pulse to the phase of the output pulse. At an input power level of 22 dBm, the phase variation during the pulse is negligible. For 24 dBm in, a phase variation of $\approx$ 1 degree can be observed during the pulse decay period. When driven hard to an input level of 26 dBm, a 6 degree phase excursion is observed during the pulse turn-off period. Note that these observed dynamic phase changes correspond well to the static transmission phase changes as shown on Figure 3. Just as important, is the absence of any jitter in the displays indicating consistent pulse-to-pulse phase behavior, an important consideration for array applications.

In order to better evaluate the class B mode of operation for array applications, an MIC single stage class B amplifier (shown in Figure 6) was designed and tested using the MGF 2124G FET. The design band was 9 to 10 GHz and class B input and output power match data was obtained from an electronic load-pull setup. In Figure 7 measured power out (P_{out}) and power added efficiency (η_{PA}) of the amplifier is plotted vs. input power at 9.5 GHz. As can be seen from the curves, 37.5% power added efficiency and 28.5 dBm power output was obtained at an input power level of 23.8 dBm (corresponding to 4.7 dB gain). Another significant feature of these curves is the large dynamic range (> 10 db) wherein both the gain varies by less than 1 db and the η_{PA} >20%. A similar amplifier operating class A could be expected to have a peak η_{PA} of between 20 and 25% and suffer a reduction of η_{PA} down to 2 or 3% over a 10 db power range.

The 180° conduction angle of class B operation results in a current waveform which is rich in even harmonics. Measurements made of the amplifier have shown that the second harmonic is down about 40 db even though no special circuits for harmonic suppression or filtering were included. Through the use of push-pull circuits and/or special harmonic rejection filters, it is expected that the second harmonic can be down 60 to 80 db below the fundamental if required.

Conclusions

In addition, to the well known class B advantages of high η_{PA} and self turn on for pulsed operation, it has been shown that class B FET amplifiers have several other important features including:

1) Significantly reduced power dissipation
2) A dynamic range of typically 8-10 db over which gain is constant and power added efficiency is > 30%.
3) Phase behavior (static and dynamic) is comparable to that observed with similar FETs operated class A.
4) Absence of erratic phase behavior during pulse turn-on and turn-off.

These features confirm the applicability of class B operation of power FET's for phased array module applications.

Advantages of Class B FET Power Amplifier

Efficiency:

		Class A	Class B	
Theoretical Upper Limits (Assume G = 5 dB)	η_{Drain}	50%	$\pi/4$ = 78.5%	
	$\eta_{P.A.} = \eta_{Drain}(1 - \frac{1}{G})$	34.2%	53.7%	
Good FET Device η_{PA} (10 GHz)		25%	40%	
Good FET Amplifier η_{PA} (10 GHz)		22%	35.2%	Down 37%
$(P_{DC})_{In}$ for $(P_{RF})_{Out}$ = 1 W		3.10 W	1.94 W	
$P_{DISS} = (P_{DC})_{In} + (P_{RF})_{In} - (P_{RF})_{Out}$		2.42 W	1.26 W	Down 48%

Figure 1

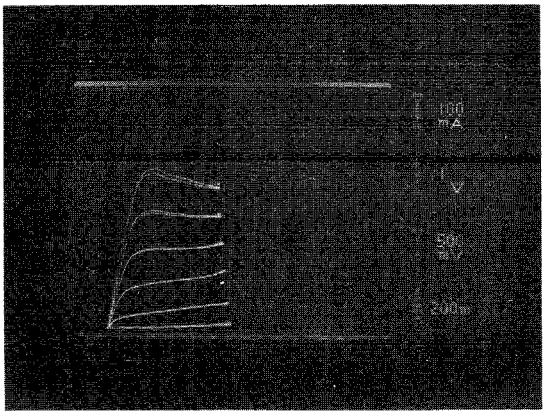

Figure 2. DC characteristics of Mitsubishi MGF 2124 FET.

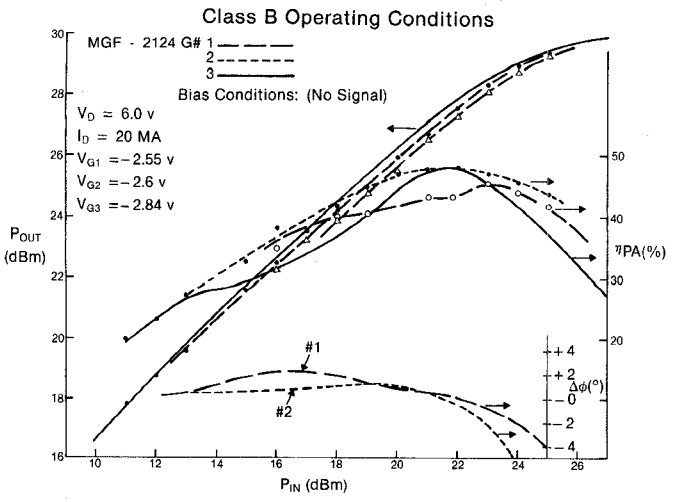

Figure 3. P_{out}, power added efficiency (η_{PA}) and transmission phase variation ($\Delta\phi$) vs. P_{in} for three MGF 2124 FETs operating class B.

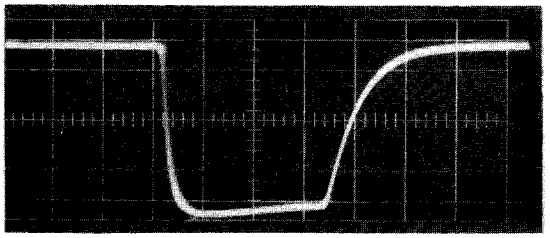

Figure 4a. Input pulse shape (Horizontal scale = 0.5 μ sec./div.) Bias (no signal) for all tests: V_D = 8V, I_D = 30 mA, V_G = -3V.

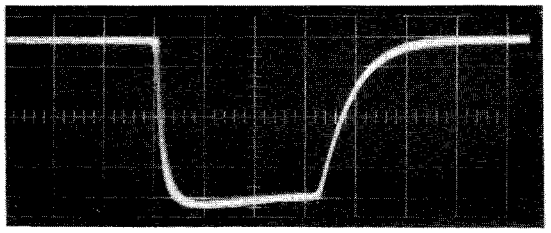

Figure 4b. Amplified pulse. P_{in} = 16 dBm

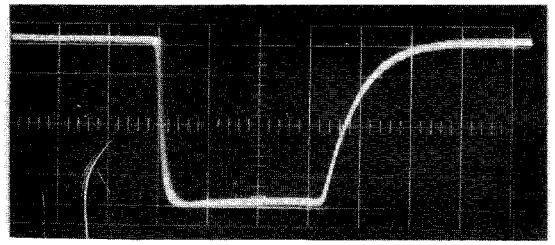

Figure 4C. Amplified pulse. P_{in} = 25 dBm

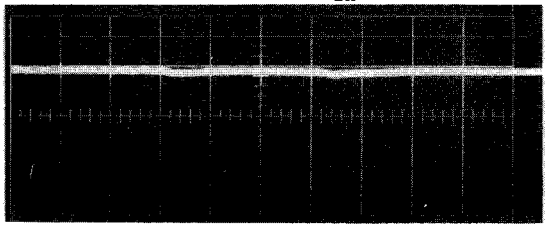

Figure 5a. Phase bridge output showing interpulse phase variation (Horizontal scale = 0.5 μsec/div., vertical scale = 4°/div.) P_{in} = 22 dBm

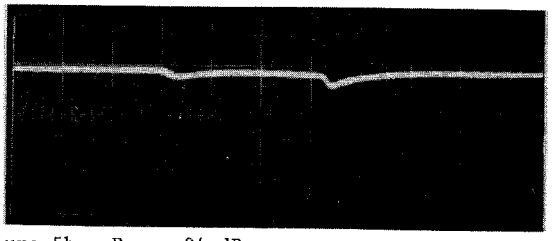

Figure 5b. P_{in} = 24 dBm

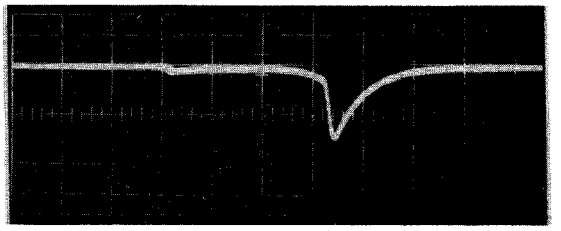

Figure 5c. P_{in} = 26 dBm

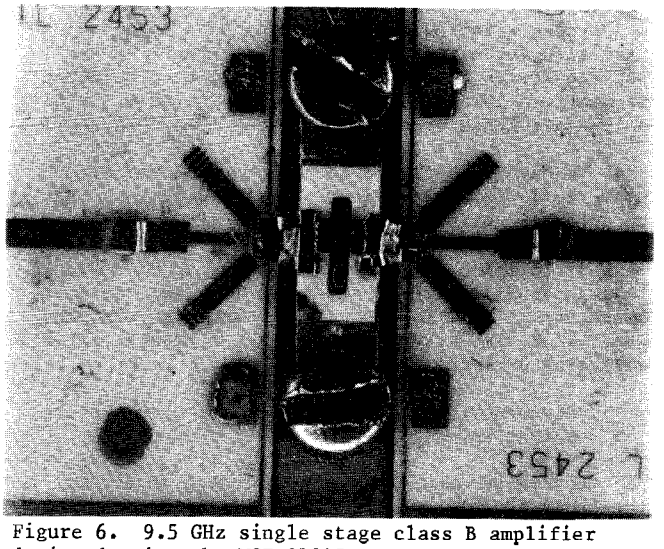

Figure 6. 9.5 GHz single stage class B amplifier designed using the MGF 2124G FET.

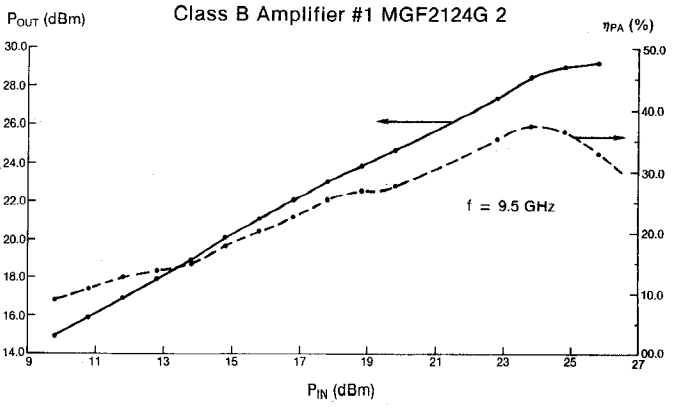

Figure 7. Measured P_{out} and power added efficiency (η_{PA}) vs. P_{in} for amplifier in Figure 6. 28.5 dBm power output (4.5 dB gain) was obtained with 37.5% power added efficiency at 9.5 GHz.